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Reg. No. : .....

Name : .....

Seventh Semester B.Tech. Degree Examination, June 2009
(2003 Scheme)
Branch : ELECTRONICS AND COMMUNICATION
03.701 : VLSI Circuit Design (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. What are the advantages of ion implantation over diffusion ?
2. What is meant by IC design rules ? With diagram, explain the rules related to wells.
3. Explain strong and weak logic levels with reference to MOSFET circuits.
4. What are the advantages of polisilicon gate over metal gate in a CMOS IC ?
5. What are the parameters on which threshold voltage of a MOSFET depend ?
6. What is hot electron effect ? How does it affect MOSFET characteristics ?
7. Derive expression for the dynamic power dissipation of a static CMOS inverter.
8. With circuit diagram explain the configuration of a 4×4 NOR-ROM array.
9. What are the functions of sense amplifier ? With circuit diagram explain the principle of a single ended sense amplifier.
10. Define the terms: observability and controllability. **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. a) With diagrams explain photolithographic process in IC fabrication.

    b) What is epitaxial layer ? Explain any one method of epitaxial growth .

12. a) Explain the sequence of operations involved in the fabrication of a CMOS inverter in self aligned polysilicon gate p well process, with diagrams.

    b) Explain the terms LDD and Channel stop implantation.

13. a) What are the advantages and disadvantages of SOI process over standard CMOS process?

    b) What are the differences between micron rule and λ rule ? Explain design rule related to metal 1 and polysilicon 1.

Module – II

14. a) Draw the circuit diagram and layout of a 4 input NAND gate in static CMOS logic. How is NAND gate superior to NOR gate in static CMOS logic ?

    b) What are the advantages and disadvantages of pass transistor logic ?

15. a) Derive the transfer characteristics of a static CMOS inverter graphically.

    b) Derive expression for the switching threshold of a static CMOS inverter.

16. a) What are the advantages and disadvantages of dynamic CMOS logic ? Explain the operation of a 3 input NAND gate in dynamic CMOS logic.

    b) How is charge leakage and charge sharing problems rectified in dynamic logic ?

Module – III

17. a) Explain the principle of an array multiplier.

    b) With circuit diagram explain a static RAM cell.

18. a) Explain the principle of operation of a carry look ahead adder. Show a CMOS implementation of a 4 bit carry look ahead generator.

    b) Draw the circuit diagram of a differential sense amplifier and explain.

19. a) Explain design for testability. What are the methods used for design for testability ?

    b) Explain the principle of an EEPROM cell. **(6×10=60 Marks)**

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