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Question Paper Code : 20108

M.E./M.Tech. DEGREE EXAMINATION, JANUARY 2011.

First Semester

VLSI Design

(Common to Applied Electronics)

252102 — VLSI DESIGN TECHNIQUES

(Regulation 2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. If you want to design a circuit using MOS transistors, which type of MOS you will preferred, whether NMOS or PMOS. Give the reason for your choice.
2. What is meant by body effect?
3. Draw the circuit diagram and briefly explain about the NMOS inverter.
4. Draw the NAND gate and NOR gate stick diagram.
5. Define the term scaling.
6. Write the importance of parasitic R, L and C calculation in the design of an IC.
7. Describe the reason for cross talk in an IC.
8. List the basic types of CMOS testing.
9. Give the differences between gate level modeling and data flow modeling.
10. Write the importance of test bench.

PART B — (5 × 16 = 80 marks)

11. (a) Describe in detail about the different MOS models and explain about the small signal AC characteristics of MOS transistor. (16)

Or

- (b) (i) Explain in detail about the second order effects in the MOS transistors. (8)
- (ii) Derive the basic design equation for a MOS transistor with the relationship between threshold voltage and body effect. (8)
12. (a) (i) Derive the expression for DC characteristics of CMOS inverter. (8)
- (ii) Discuss the design techniques to reduce switching activity in a dynamic CMOS circuits. (8)

Or

- (b) (i) Analyze the CMOS inverter circuit with driving the large capacitance loads. (8)
- (ii) What is meant by transmission gate? List the applications of transmission gates and design a 2×1 multiplexer operation circuit using transmission gates. (8)
13. (a) (i) Explain in detail about the charge sharing concept and design margin concepts. (12)
- (ii) Write short notes about the transistor sizing for the performance in combinational Networks. (4)

Or

- (b) Describe in detail about the resistance and capacitance estimation calculation in a CMOS circuit with the proper loads and drivers. (16)
14. (a) Explain in detail about any three types of adders. (16)

Or

- (b) (i) Explain in brief about the architecture design for multipliers. (8)
- (ii) Explain in detail about the pipeline concepts used in sequential circuits. (8)
15. (a) (i) Write a data-flow model verilog HDL program for the two input comparator circuit. (8)
- (ii) Write a behavioral level verilog HDL program for the 1×8 multiplexer circuit. (8)

Or

- (b) Write a behavioral model verilog HDL program for the ripple carry adder circuit. (16)