Code No: RR220203 **Set No. 1**

II B.Tech II Semester Supplimentary Examinations, Apr/May 2008
LINEAR AND DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Why is it necessary to use an external offset voltage compensating network with practical OP-AMP circuits?
   (b) Compare and contrast an ideal OP-AMP and practical OP-AMP.
   (c) Explain the precautions that can be taken to minimize the effect of noise on an OP-AMP circuit.
   (d) Calculate the effect of variation in power supply voltages on the output offset voltage for an inverting amplifier circuit. [6+4+2+4]

2. (a) List and explain the two special cases of inverting amplifiers. [6]
   (b) What is a voltage follower? What are its features and applications? [4+6]

3. (a) Discuss the functioning of a practical integrator and derive the necessary expressions. [4+4]
   (b) Design a practical integrator circuit to properly process input sinusoidal waveforms upto 1 KHz. The input amplitude is 10mV. [8]

4. (a) Draw the circuit of Schmitt trigger using 555 timer and explain its operation. [2+6]
   (b) How is an Astable multivibrator using 555 timer connected in to a pulse position modulator? [8]

5. (a) Give the functional block diagram of NE 565 PLL (DIP) and for the given component values. $C_1 = 390PF$, $C_2 = 680PF$ and $R_1 = 10k$, $V_{cc} = \pm 6V$ Find:
      i. The free running frequency
      ii. The lock range and capture range.

      Where C_1 is the capacitor connected between pin number 9 and $-V_{CC}$, C_2 is the capacitor connected between $+V_{CC}$ and output pin 7, and R_1 is connected between pin number 8 and $+V_{CC}$
   (b) Give the functional block diagram of VCO NE566 and explain its working and necessary expression for free running or center frequency. [8+8]

6. (a) Explain the term ''Frequency Sealing'' with suitable example.
   (b) Design a wide band-pass filter with f_L=200Hz. F_H=1KHz and a pass-band gain=4. Draw the frequency response and calculate 'Q' factor for the filter. [6+10]

7. (a) Define:
   i. Positive logic
   ii. Negative logic
   iii. Pulse logic.
   (b) What is meant by AOI logic. Explain with help of an example.
   (c) In the given circuit (figure 7) silicon transistor is used. Find the out-put levels for the given input levels of 0.2V and 12V, obtained from a preceding stage. Assume h_{FE}=30. [6+5+5]

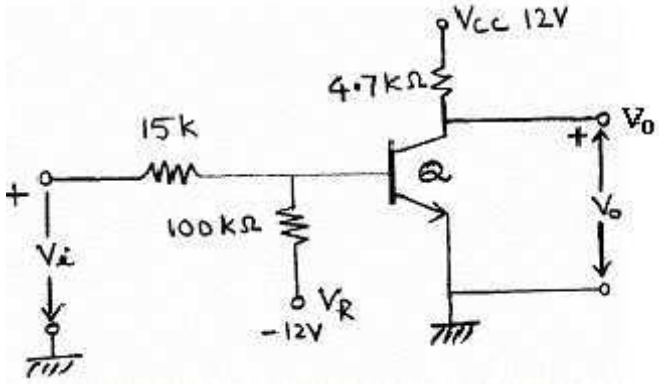

Figure 7

8. (a) Compare different A/D converters for their merits and demerits.
   (b) Give the schematic circuit diagram of a successive approximation type A/D converter and explain the operations of this system. [8+8]

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Code No: RR220203 **Set No. 2**

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1. (a) Define the terms: SVRR,CMRR, input bias current, input offset voltage,Gain Bandwidth product.
   (b) What are the differences between the inverting and non inverting terminals? What do you mean by the term "virtual ground"? [10+6]
2. (a) Derive the closed loop voltage gain, input resistance, output resistance and bandwidth for an inverting amplifier with feedback arrangement.
   (b) Briefly explain why negative feedback is desirable in amplifier applications. How does negative feedback affect the performance of an inverting amplifier? [8+8]
3. (a) Briefly describe three uses of an analog multiplier. [8]
   (b) What do you mean by sampling? Explain the basic circuit for sample and hold circuit. [2+6]
4. (a) Draw the circuit of Schmitt trigger using 555 timer and explain its operation. [2+6]
   (b) How is an Astable multivibrator using 555 timer connected in to a pulse position modulator? [8]
5. (a) Draw the circuit of a PLL AM detector and explain its operation.
   (b) What is the major difference between digital and analog PLLs? [8+8]
6. (a) Explain the term "VSVS configuration". Design a VCVS low-pass Butterworth second order filter with a cutoff frequency of 4 kHz. Assume necessary data in the design process.
   (b) Design a second order IGMF band-pass filter with the following specifications : f_o=500 Hz; Gain at resonance=-5 and band-width=50Hz. Use the circuit shown below (figure 6). Assume necessary data. [8+8]

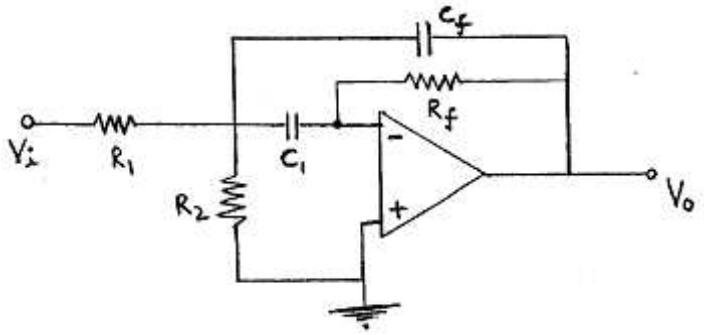

Figure 6

7. For the circuit shown below (figure 7)

   (a) Explain the operations and the circuit with the help of Truth-Table.

   (b) If h_{FE} of Q_1 is 30, find h_{FE}min of Q_2.

   (c) If h_{FE} of Q_2 is 30, what is Fan-Out?

   (d) Find Noise Margins. [4×4]

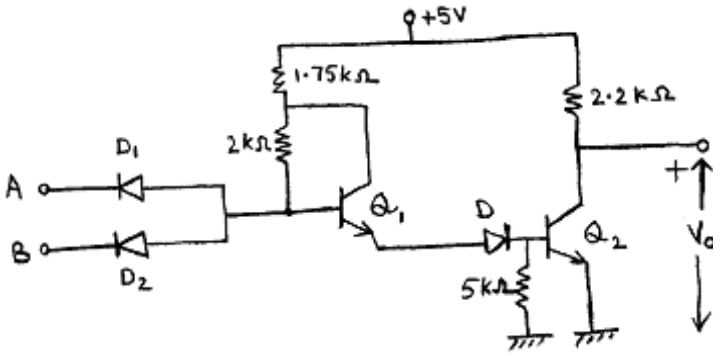

Figure 7

8. (a) Draw the schematic circuit diagram of 4 bits Successive Approximations A/D converter and explain its operation.

   (b) Compare this A/D converter with parallel comparator type A/D converter.

   (c) Give the working principle of analog multiplexer. [6+5+5]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Define the terms: SVRR,CMRR, input bias current, input offset voltage,Gain Bandwidth product.
   (b) What are the differences between the inverting and non inverting terminals? What do you mean by the term "virtual ground"? [10+6]

2. (a) Draw the circuit and explain the working of:
      i. voltage to current converter
      ii. current to voltage converter. [2×4]
   (b) Draw a circuit using Op-Amp, which can work as adder (inverting and non-inverting) and explain how it works. [2×4]

3. (a) Briefly describe three uses of an analog multiplier. [8]
   (b) What do you mean by sampling? Explain the basic circuit for sample and hold circuit. [2+6]

4. (a) Draw the circuit of Schmitt trigger using 555 timer and explain its operation. [2+6]
   (b) How is an Astable multivibrator using 555 timer connected in to a pulse position modulator? [8]

5. (a) What are the important blocks of PLL. What is the role of each block? Explain in detail.
   (b) Give any two applications of PLL and explain about each applications in detail. [8+8]

6. (a) Derive the transfer function for a general second order sallen-key filter with suitable circuit diagram.
   (b) Design a Butterworth filter for a given normalized polynomial of S^2+1.414S+1. Assume necessary data. [8+8]

7. For the given circuit shown below (figure 7d):
   (a) Explain the operations of the circuit with the help of Truth-Table.
   (b) If h_{FE} of Q_1 is 30, find h_{FE}min of Q_2
   (c) If h_{FE} of Q_2 is 30, what is Fan-Out?

(d) Find Noise-Margin. [4×4]

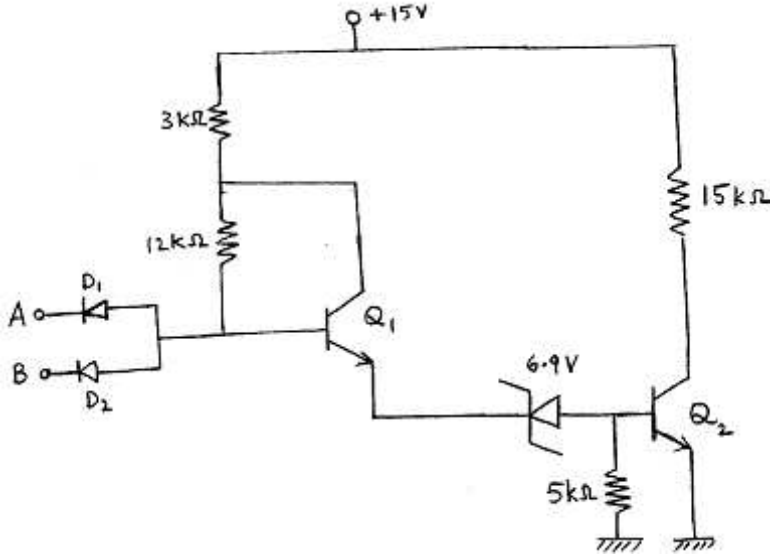

Figure 7d

8. (a) List out different types of A/D converters.
   (b) Draw the schematic circuit diagram of dual-slope A/D converter and explain its operation. Derive expression for output voltage.
   (c) Compare dual-slope A/D converter with successive approximation A/D converter. [6+5+5]

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Code No: RR220203 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Give the design procedure of a compensating network for an OP-AMP which uses ±10V supply voltages. Assume necessary data.
   (b) In the circuit of figure1b below, R_1=100Ω, R_F=4.7KΩ CMRR=90 db. If the amplitude of the induced 60-Hz noise at the output is 5mv (rms), calculate the amplitude of the common-mode input voltage $V_{cm.}$. [8+8]

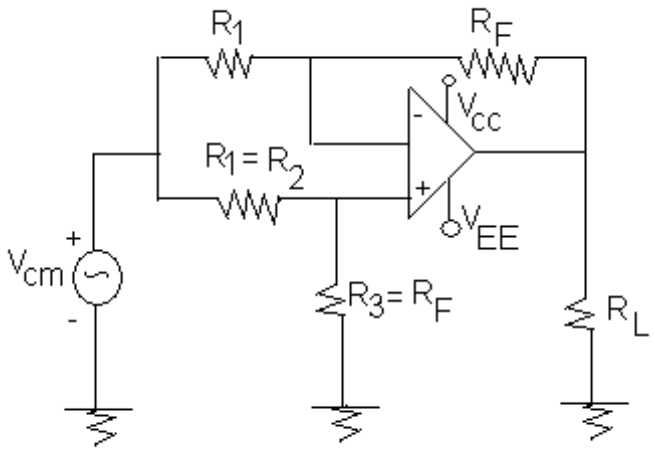

Figure 1b

2. (a) Explain the operation of Zero crossing detector.
   (b) Briefly mention the disadvantages of using Zero crossing detector and how it is overcome in Schmitt Trigger? [8+8]

3. (a) Briefly describe three uses of an analog multiplier. [8]
   (b) What do you mean by sampling? Explain the basic circuit for sample and hold circuit. [2+6]

4. (a) Explain the significance of each of comparators and operation of 555 timer. [3+5]
   (b) Explain the application of 555 timer as Linear ramp generator. [8]

5. (a) What is the major difference between digital and analog PLLs?
   (b) Explain the frequency multiplier using IC PLL. [8+8]

6. (a) Explain the operation of a delay equalizer circuit with neat sketches. Derive an expression relating input and output voltages of the equalizer.
   (b) For the all pass filter, determine the phase shift between input and output at f=2 kHz. To obtain a positive phase shift. What modifications are necessary in the circuit? [8+8]

7. For the given circuit explain its operation with the help of Truth Table. Find h_{FE}min, Fan-out if h_{FE}=30, and Noise-Margin for the given circuit shown below(figure 7). (Assume all the active devices are made of silicon). [16]

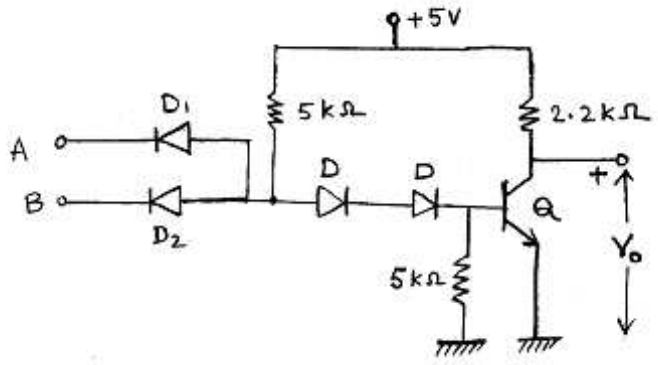

Figure 7

8. (a) Draw the circuit of a Weighted Resistor DAC and obtain expression for n-bits.
   (b) Sketch the Analog output voltage for the given digital input code.
   (c) What are the major disadvantages in this type? [6+5+5]

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