

IV B.Tech I Semester Supplementary Examinations, November 2006
FAULT TOLERANT SYSTEMS

(Common to Computer Science & Engineering and Electronics &
 Computer Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) A computer system contains 10,000 components each with failure rate 0.5% per 1000 hours. What is the period of 0.99 reliability of this system.
 (b) What is meant by active repair time and passive repair time referred in maintainability of a system. Derive the expression for the MTTR. [6+3+3+4]
2. (a) A circuit realizes the function.

$$Z = \overline{X_1} X_4 + \overline{X_2} X_3 + X_1 \overline{X_4}$$
 Using Boolean Difference method find the test vectors for SA0, SA1 faults on all input lines of the circuit.
 (b) What are the different properties of Boolean differences? Explain [5+5+6]
3. Derive the Reliability factor of TMR and Triplicated TMR systems. Show that R(t) of Triplicated TMR is better than R(t) of TMR system. [5+5+6]
4. (a) Explain in detail the practice fault Tolerant space shuttle computer complex system.
 (b) What are the different ways to have software redundancy. [8+8]
5. (a) Write short notes on
 - i. Fault secure circuit
 - ii. Self-testing circuit
 - iii. Code disjoint circuit
 (b) Write short notes on:
 - i. self-checking circuit
 - ii. self-checking checker circuit
 - iii. fail safe circuit [8+8]
6. (a) Explain the advantages of PLA and how it is used as totally self-checking circuit.
 (b) For the given 4 input, 4 output function design a totally self checking checker circuit using PLAs. [6+10]

$$f_1(A,B,C,D) = \sum (0,2,3,7,8,10,12,13,15)$$

$$f_2(A,B,C,D) = \sum (0,2,3,4,9,12,13,15)$$

$$f_3(A,B,C,D) = \sum (0,1,2,4,8,9,10,14)$$

$$f_4(A,B,C,D) = \sum (0,1,2,4,5,6,8,11,14).$$

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7. (a) What are the goals of a design for testability?
(b) What are the different DET methods available? Explain at least two such techniques. [6+4+6]
8. Explain observability enhancement with neat diagram with suitable examples. [4+2+10]
