

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER-III (New) EXAMINATION – WINTER 2015

Subject Code:2131704

Date:18/12/2015

Subject Name: Digital Logic Circuits

Time: 2:30pm to 5:00pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		MARKS																																								
Q.1	Short Questions	14																																								
1	Convert $(B65F)_{16}$ to decimal	1																																								
2	$F = x y + x' y' + y' z$ implement with gates	1																																								
3	Draw vein diagram for AND gate	1																																								
4	Determine the values of A, B, C, and D that make the sum $\bar{A} + B + \bar{C} + D$	1																																								
5	Derive the Boolean expression for the logic circuit shown below:	1																																								
6	From the truth table below, determine the standard SOP expression.	1																																								
	<table border="1" style="border-collapse: collapse; text-align: center; width: 150px; margin: auto;"> <thead> <tr> <th colspan="3">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	Inputs			Output	A	B	C	X	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1	1	1	0	0	0	1	0	1	0	1	1	0	1	1	1	1	0	
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7	Convert the binary number 1001.0010_2 to decimal.	1																																								
8	Define Flip Flop	1																																								
9	Applying DeMorgan's theorem to the expression \overline{ABC} , we get _____.	1																																								
10	An AND gate with schematic "bubbles" on its inputs performs the same function as a(n) _____ gate.	1																																								
11	A truth table for the SOP $AB\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$ expression has how many input combinations?	1																																								
12	$AC + ABC = AC$, say whether True or False	1																																								
13	Converting the Boolean expression $LM + M(NO + PQ)$ to SOP form, we get _____	1																																								
14	Prove $x+x=x$ using theorems and postulates																																									
Q.2	(a) Simplify: $A'B + A'BC' + A'BCD + A'BC'D'E$	03																																								

	(b)	Implement $F = A(B + CD) + BC'$ with NOR gate	04
	(c)	Simplify the following Boolean function in a) Sum of Products and b) Product of Sums: $F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$	07
		OR	
	(c)	Prove that: 1. $((AB' + ABC)' + A(B + AB'))' = 0$ 2. $AB'C + A'BC + ABC = AC + AB$	07
Q.3	(a)	State and prove De-Morgan's theorem	03
	(b)	Explain Half adder	04
	(c)	Construct 4x16 decoder with two 3x8 decoders.	07
		OR	
Q.3	(a)	Express following Function in Product of Maxterms $F(x,y,z) = (xy + z)(y + xz)$	03
	(b)	Explain Master Slave Flip Flop using J.K Flip Flop	04
	(c)	Simplify the Boolean Function: $F(w,x,y,z) = \sum(1,3,7,11,15)$ and the Don't care conditions : $d(w,x,y,z) = \sum(0,2,5)$	07
Q.4	(a)	Explain combinational logic circuit and sequential logic circuit.	03
	(b)	Write a note on clocked RS flip flop	04
	(c)	Simplify the Boolean function using the tabulation method $F(A,B,C,D,E,F,G) = \sum(20,28,38,39,52,60,102,103,127)$	07
		OR	
Q.4	(a)	Explain TTL circuit in detail	03
	(b)	List and explain at least two characteristics of Logic families in detail.	04
	(c)	With block diagram explain Successive approximation ADC.	07
Q.5	(a)	Explain ALU	03
	(b)	Explain Registers.	04
	(c)	With logic circuit explain the working of 4-bit magnitude comparator.	07
		OR	
Q.5	(a)	Realize AND and NOT gate using NOR gate	03
	(b)	Explain state table, state diagram with example	04
	(c)	Design a 3-bit binary counter using JK Flip-Flop	07
