Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (New) EXAMINATION – WINTER 2015

Subject Code:2132003 Date:18/12/2015

Subject Name: Design Concepts In Basic Electronics

Time: 2:30pm to 5:00pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** **14**

1 Convert (3254.64)8 into equivalent Binary and Hexadecimal.

2 Following arithmetic operation is correct for the base x. Find base x.

$$(21)_x + (44)_x + (32)_x + (13)_x = (143)_x$$

3 Represent $(786)_{10}$and $(75)_{10}$ in equivalent BCD and add them showing BCD arithmetic.

4 If we want to implement 2 function at the same time what must be used out of decoder and multiplexer for the implementation.

5 Why look ahead carry generator is required?

6 Explain the importance of Gray code.

7 State points of difference between BCD and binary code.

8 Define peak inverse voltage of diode

9 What do you mean by ideal diode?

10 Why a filter circuit is required after rectifier?

11 What are the parameter on which current gain of transistor depends?

12 With help of output curve of transistor explain load line and Q point.

13 If transistor is to be operated as switch where must be the Q point located.

14 What is voltage multipliers?

Q.2 **(a)** With circuit diagram and output waveform explain working of full wave bridge rectifier **03**

(b) Give the points of difference between half wave, Full wave, and Bridge rectifier. **04**

(c) Simplify the following Boolean function using Karnaugh map method and realize with minimum NOR gates only. **07**

F (A,B,C,D) = ∑ (0,1,3,7,13,15)+ d (2,11,12,14)

OR

(c) Design a combinational logic to convert given BCD to seven segment display LED. **07**

Q.3 **(a)** Draw and explain internal construction of encoder. **03**

(b) Implement the following function with help of 8x1 Multiplexer. **04**

F (A,B,C,D) = ∑ (0,1,3,4,8,9,15)

(c) Compare in detail RTL, DTL, TTL, ECL and CMOS. **07**

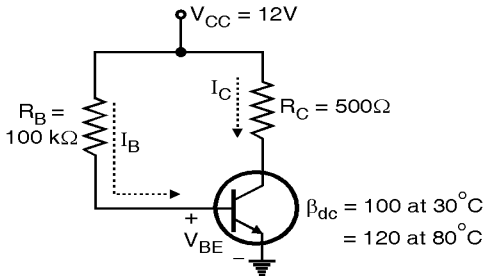
OR

Q.3 **(a)** Write the points of difference between combinational and sequential logic. **03**

	(b)	Draw the circuit diagram of D-type positive edge triggered flip flop	**04**
	(c)	Write a note on collector to base bias.	**07**
Q.4	**(a)**	What is ripple counter?	**03**
	(b)	Explain in detail bidirectional shift register with parallel load	**04**
	(c)	Discuss with example approximate analysis of the voltage divider bias.	**07**

OR

Q.4	**(a)**	Why we require master slave or edge triggered flip flop	**03**
	(b)	Design 3- bit up synchronous counter.	**04**
	(b)	Write the points of comparison between CB, CE and CC configuration of transistor.	**07**
Q.5	**(a)**	What is energy band diagram?	**03**
	(b)	Explain the different types of clipping circuits	**04**
	(c)	The fixed bias circuit of Fig. uses a silicon transistor. The component values are RC = 500 Ω and RB = 100 kΩ. βdc of the transistor is 100 at 30°C and increases to 120 at a temperature of 80°C. Determine the percent change in the Q point values over this temperature range. Assume that VBE and ICBO remain constant.	**07**



OR

Q.5	**(a)**	Explain the requirement of compliment in digital logic.	**03**
	(b)	Explain with circuit diagram positive clamper and negative clamper.	**04**
	(c)	Explain DC load line and Q-point for any transistor configuration. Also state the necessity of biasing and list biasing methods for transistor	**07**

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