Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER – VIII.EXAMINATION – WINTER 2016

Subject Code: 180802 Date: 20/10/2016

Subject Name: VLSI Technologies

Time: 02:30 PM to 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Why drop occurs in a MOSFET? What is threshold voltage? Derive expression of V_{th}. **07**

(b) Explain VLSI design flow (Y- chart) in detail. **07**

Q.2 **(a)** Describe CMOS fabrication (n-well) process with neat and clean diagram. **07**

(b) Draw and explain VTC of MOS inverter. Derive expression of I_D. **07**

OR

(b) Explain gradual channel approximation. Derive expression of I_D and I_D by considering channel length modulation. **07**

Q.3 **(a)** Explain BIST method for chip testing. **07**

(b) What is voltage Bootstrapping? Derive the expression of V_x. **07**

OR

Q.3 **(a)** Explain Ad-Hoc testable technique for chip testing. **07**

(b) What is latch-up? List and explain its causes and preventions. **07**

Q.4 **(a)** Explain and derive expression for CMOS NAND2 gate. **07**

(b) Calculate the threshold voltage V_{T0} at V_{SB} = 0v, for a polysilicon gate n-channel MOS transistor, with the following parameters: Substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox} = 500A° and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}. **07**

Assume: ϕ_F(Gate) = 0.55V, $n_i = 1.45 \times 10^{10}$ cm^{-3}, thermal voltage (kT/q) = 0.026

OR

Q.4 **(a)** Write a detailed note on high performance Dynamic CMOS logic **07**

(b) Consider a resistive-load inverter circuit with V_{DD} = 5v, $k'_n = 20\mu A/V^2$, V_{T0} = 0.8v, R_L = 200K and (w/l) = 2. Calculate the critical voltages (V_{OH}, V_{OL},V_{IL} & V_{IH}) and find the noise margins of the circuit. **07**

Q.5 **(a)** What are pass transistor circuits? Explain logic '0' and logic '1' transfer. **07**

(b) Explain switching power dissipation of CMOS inverter. Derive power delay expression. **07**

OR

Q.5 **(a)** What are CMOS transmission gates? Explain its region of operation. **07**

(b) Compare and list out difference between FPGAs and CLPDs. **07**

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