Roll No. .....

BCA-11/BA-IT-12 (Bachelor of Computer Applications)

Fourth Semester Examination-2015

BCA-11

Computer Organization

Time : 3 Hours **Maximum Marks :** 60

Note : This paper is of sixty (60) marks divided into three (03) sections A, B, and C. Attempt the questions contained in these sections according to the detailed instructions given therein.

Section - A

(Long Answer Type Questions)

Note : Section 'A' contains four (04) long-answer-type questions of fifteen (15) marks each. Learners are required to answer any two (02) questions only. (2×15=30)

1. With truth table and logic diagram explain the working of a Full-adder circuit.

2. What do you mean by addressing mode? Discuss the different addressing mode of 8085 with example.

3. (a) With a neat block diagram, show how the basic computer registers are connected to the common bus.

   (b) With a neat diagram, explain the instruction pipeline processing in RISC architecture.

4. What do you mean by cache coherence? Mention the condition where which cache coherence occurs. Explain, how cache coherence problem can be resolved.

Section - B

(Short Answer Type Questions)

Note : Section 'B' contains eight (08) short-answer-type questions of five (05) marks each. Learners are required to answer any four (04) questions only. (4×5=20)

1. Draw the block diagram of single-bus organization of the data paths inside the CPU.

2. Draw the block diagram of a DMA controller explain its functioning.

3. Differentiate between hardwired & micro-programmed Computers.

4. Compare synchronous counters with asynchronous counters.

5. What is the function of a Multiprocessor system and list out the various characteristics of Multiprocessors?

6. Draw the instruction word format and indicate the number of bits in each part.

7. What is the dierence between microprocessor and micro program? Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessors?

8. Write a short notes on Demultiplexer.

Section - C

(Objective Type Questions)

Note : Section 'C' contains ten (10) objective-type questions of one (01) mark each. All the questions of this section are compulsory. (10×1=10)

1. A source program is usually in ..... .

   a) Assembly language b) Machine level language

   c) High-level language d) Natural language

2. The ALU makes use of ..... to store the intermediate results.

   a) Accumulators b) Registers

   c) Heap d) Stack

3. In memory-mapped I/O ...

   a) The I/O devices and the memory share the same address space

   b) The I/O devices have a seperate address space

   c) The memory and I/O devices have an associated address space

   d) A part of the memory is specifically set aside for the I/O operation

4. The addressing mode, where you directly specify the operand value is ..... .

   a) Immediate b) Direct

   c) Definite d) Relative

5. The decoded instruction is stored in .....

a) IR b) PC

c) Registers d) MDR

6. Which of the register/s of the processor is/are connected to Memory Bus?

a) PC b) MAR

c) IR d) Both a and b

7. ..... bus structure is usually used to connect I/O devices.

a) Single bus b) Multiple bus

c) Star bus d) Rambus

8. PROM stands for

a) Programmable Read Only Memory.

b) Pre-fed Read Only Memory.

c) Pre-required Read Only Memory.

d) Programmed Read Only Memory.

9. The read and write operations usually start at ..... of the sector.

a) Center b) Middle

c) From the last used point d) Boundaries

10. The control unit controls other units by generating ..... .

a) Control signals b) Timing signals

c) Transfer signals d) Command Signals