

**GUJARAT TECHNOLOGICAL UNIVERSITY**  
**BE – SEMESTER – VI (OLD).EXAMINATION – WINTER 2016**

**Subject Code: 161004****Date: 25/10/2016****Subject Name: VLSI Technology and Design****Time: 10:30 AM to 01:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

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|------------|-----|--|-----------|
| <b>Q.1</b> | (a) | Explain VLSI design flow.                                      | <b>07</b> |
|            | (b) | Describe fabrication process of MOSFET.                        | <b>07</b> |
| <b>Q.2</b> | (a) | Write short note on Fault types and models.                    | <b>07</b> |
|            | (b) | Write short note on On Chip Clock Generation and Distribution. | <b>07</b> |
|            |     | <b>OR</b>  |           |
|            | (b) | Write short note on FPGA.                                      | <b>07</b> |
| <b>Q.3</b> | (a) | Write short note on Layout Design rules.                       | <b>07</b> |
|            | (b) | Explain CMOS inverter in detail.                               | <b>07</b> |
|            |     | <b>OR</b>  |           |
| <b>Q.3</b> | (a) | Write short note on resistive load Inverter.                   | <b>07</b> |
|            | (b) | Write short note on MOS Inverters Switching characteristics.   | <b>07</b> |
| <b>Q.4</b> | (a) | Write short note on CMOS Transmission Gates.                   | <b>07</b> |
|            | (b) | Explain Basic Principles of pass transistor circuits.          | <b>07</b> |
|            |     | <b>OR</b>  |           |
| <b>Q.4</b> | (a) | Write short note on CMOS Edge-triggered flip-flop.             | <b>07</b> |
|            | (b) | What is latch-up? How to prevent it?                           | <b>07</b> |
| <b>Q.5</b> | (a) | Write short note on SR latch.                                  | <b>07</b> |
|            | (b) | Implement $F = AB + C'D(A'+B')$ using CMOS logic circuits.     | <b>07</b> |
|            |     | <b>OR</b>  |           |
| <b>Q.5</b> | (a) | Write short note on CPLD.                                      | <b>07</b> |
|            | (b) | Write short note on built-in Self Test (BIST) techniques.      | <b>07</b> |

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