PART B — (5 × 16 = 80 marks)

11. (a) (i) List the features of DTL logic family and explain the function of DTL NAND gate. (8)

(ii) Explain the function of TTL logic with totem pole output configuration. (8)

Or

(b) Explain in detail the CMOS logic circuits and CMOS transmission gates. (16)

12. (a) (i) Explain the Full subtractor. (6)

(ii) Explain the 4 bit Adder - Subtractor using parallel load. How the detection of overflow is verified? (10)

Or

(b) (i) Explain the function of Carry look ahead adder. (8)

(ii) Draw and Explain the 3 bit Magnitude comparator. (8)

13. (a) (i) Explain the function of Demultiplexer and Parity checker. (8)

(ii) Describe the Binary to Gray code converter. (8)

Or

(b) (i) Implement the Boolean function $F(x,y,z)= \Sigma(1,2,6,7)$ using Multiplexer. (8)

(ii) Discuss about the basics of different modeling methods. Write a Dataflow model for a 4 bit adder. (8)

14. (a) (i) Draw and Explain the block diagram of Moore and Mealy state machines. (8)

(ii) Describe the ASM chart and explain the application of the ASM chart to design a sequential circuit with an example. (8)

Or

(b) (i) Explain the function of a universal shift register. (8)

(ii) Explain the function of Ring counter. (8)

15. (a) (i) Explain the primitive flow table and the reduction method. (8)

(ii) Discuss about Races and Cycles. (8)

Or

(b) Discuss in detail the Hazards and Hazard elimination. (16)