Electronics & Communication Engineering Department
B.E. 2nd Year (EC, EI, EE, CT)
EC001 Digital Electronic Circuits (10th Dec, 2006)
End Semester Exam

(43)

Time: 180 min **Marks: 36**

Note: 1. *Q No. 1 is compulsory*. Attempt any 4 questions from Q No.2 to Q No.6 only.
2. First five attempted questions will be checked including Q No.1.
3. Attempt all the parts of the question at one place and all questions in sequence only.
4. Draw neat and labeled circuit diagrams wherever necessary.
5. You can see end semester answer sheets on 15th Dec, 2006 in Dec lab at 12.30pm.

S No.			Marks
1	a)	Express the following function in sum of minterms and product of maxterms. $F(A, B, C, D) = \overline{B}D + \overline{A}D + BD$	2
	b)	Simplify the following Boolean expression $(x + y)(\overline{\overline{x}(\overline{y} + \overline{z})}) + \overline{x}\overline{y} + \overline{x}\overline{z}$	2
	c)	Simplify the following expressions using K- map technique. (i) $\overline{A}B + ABD + A\overline{B}C\overline{D} + BC$ (ii) $AB + A\overline{C} + AD + A\overline{B}C + ABC$	2
	d)	Perform the following (i) 247.6 + 359.4 in XS-3 code. (ii) 679.6 – 885.9 in BCD by 9's complement method.	2
2	a)	Simplify the following Boolean function using QM method $F(A, B, C, D) = \Sigma m(1,2,3,5,9,12,14,15) + d(4,8,11)$	3 2
	b)	A circuit receives a 4-bit excess–3 codes. Design a minimal circuit to detect the decimal numbers 0, 1, 4, 6, 7, 8.	2
	c)	A binary ripple counter is required to count up to $(16,383)_{10}$. How many FFs are required? If the clock frequency is 8.192MHz, what is the frequency at the output of the MSB?	
3	a)	Implement the following Boolean function with a 4 X 1 MUX and external gates. Connect inputs A and B to selection lines. $F(A, B, C, D) = \Sigma m(1,3,4,11,12,13,14,15)$	3
	b)	Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include the enable input.	2
	c)	Design a combinational circuit that accepts 3-inputs and produce its 1's complement as output. Implement the circuit using ROM.	2
4	a)	Design a divide-by-2 circuit using D flip-flop.	2
	b)	Design a MOD-6 ripple counter using JK flip-flops.	3
	c)	Convert T flip-flop to JK flip-flop.	2
5	a)	Design a type D counter that goes through states 0,1,2,4,0……. The unused states must always go to 000 on the next clock pulse.	3
	b)	Design a sequence detector which produces an output z=1 when the sequence 1111 is detected. Implement using T flip-flops.	4
6	a)	Show the circuit of a 4-input NAND gate using CMOS transistors.	2
	b)	Totem pole outputs should not be tied together to form wired logic. Comment.	2
	c)	Prove that two open collector TTL inverters when connected together, produce the NOR function.	3

**********BEST OF LUCK**********