B.E. (EE) Part-III 5th Semester Examination, 2007

S. S. Devices & Ckts.-II

(EE-503)

Time : 3 hours **Full Marks : 100**

Use separate answerscript for each half.
Answer SIX questions, taking THREE from each half.
Two marks are reserved for neatness in each half.

FIRST HALF

1. How does the bootstrapping technique increase the input resistance of a CC BJT amplifier? How can the circuit for Darlington BJT CC amplifier in Fig.-1 be modified to incorporate bootstrapping circuit?

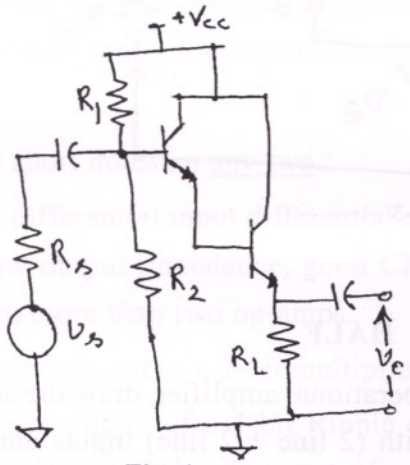

Fig.-1

If $R_1 // R_2 = 500\ k\Omega$, $R_L = 5\ k\Omega$, $h_{fe1} = h_{fe2} = 50$, $h_{ie1} = h_{ie2} = 1.5\ k\Omega$ and $1/h_{oe1} = 1/h_{oe2} = 20\ k\Omega$, find the value of the input resistance R_i without and with bootstrapping circuit. State any assumptions you have made. **[5+5+3+3]**

2. A CC circuit is shown in Fig.-2. Find the voltage gain A_v, input resistance R_{if} with feedback, the output resistance R_{of} with feedback using the concept of feedback amplifier. Given $h_{ie} = 1\ k\Omega$, $h_{fe} = 100$, $1/h_{oe} = 50\ k\Omega$ and $R_L = 1\ k\Omega$. Biasing circuit is not shown. **[6+5+5]**

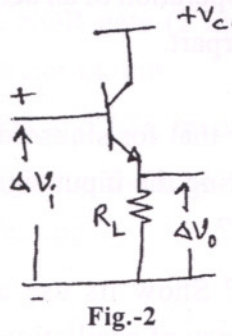

Fig.-2

3. a) Show the basic configuration of a resonant circuit sinusoidal oscillator with feedback.
   b) If all the resonant circuit elements are reactive, find at what frequency the circuit will oscillate.
   c) Under what conditions does the configuration reduce to a Colpitts Oscillator?

[6+5+5]

4. Design a transformer coupled class-B power amplifier to deliver 30 W to a load resistance $R_L = 4$ ohms. Given $V_{ce\,max} = 80\,V$, $h_{fe} = 100$ and $h_{ie} = 100\,\Omega$. Find also the power amplification of the amplifier. How do you modify this circuit to reduce cross-over distortion? **[10+3+3]**

5. For a series regulator as shown in Fig.-3, find the rating of the series transistor and the resistance R_D. Given $V_i = 18\,V \pm 2\,V$, nominal output voltage equals to 12 V the output current variation from 50 mA to 200 mA, $h_{fe} = 50$ and $h_{ie} = 100\,\Omega$ at $I_c = 200$ mA, $r_z = 12$ ohms, V_z can vary between 12.6 V to 11.4 V, nominal $V_z = 11.7$ V. Zener can dissipate 500 mW maximum and $h_{fe\,max} = 130$. Consider source resistance $R_s = 0$. Find also R_o and S_v. **[10+3+3]**

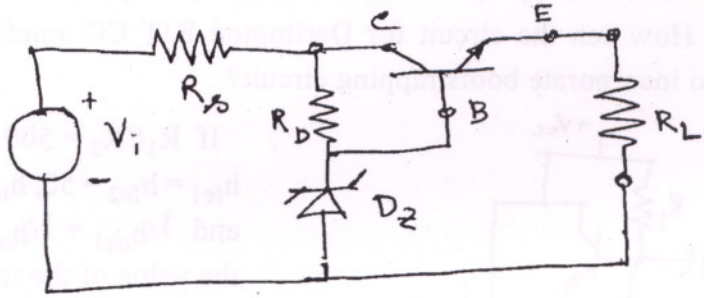

Fig.-3

SECOND HALF

6. a) With an introduction to the ideal operational amplifier, draw the adder-cum-subtracter circuit using op.amp with (2 line + 2 line) inputs and show the deduction of input-output relation.

   b) With the help of a circuit diagram, explain the operation of an active integrator circuit and compare it with its passive counterpart. **[8+8]**

7. a) What is an analog comparator circuit? Show that for sinusoidal input, this circuit gives a square-wave output by comparing the input signal to ground potential. What is another name of the circuit?

   b) What is a regenerative comparator circuit? Show its use as an astable multivibrator and the expression of its frequency of oscillation. **[8+8]**

8. a) The output (Y) of a digital system is expressed as follows, with usual notation, –

   $$Y(A, B, C, D) = \sum m\,(0, 2, 6, 9, 11, 13) + d\,(4, 5, 7, 8, 10)$$

   Use Karnaugh map and minimise the I/O relation for realisation through NAND-NAND configuration.

b) With the help of circuit diagram, develop a 2-bit comparator circuit with three-bit output Y_0, Y_1, Y_2.
Y_0 = '1', if two input words (A, B) are qual, otherwise '0'
Y_1 = 1, if word-A is greater than word-B, otherwise '0'
Y_2 = 1, if word-B is less than word-B, otherwise '0'
Note that Y_2 is to be developed using Y_0 and Y_1. [8+8]

9. a) With the help of block diagrams; truthtable; Venn diagrams; Karnaugh maps and minterm expressions and maxterm expressions of the output of a full adder circuit. Show that the full adder circuit can be realised using two half adders. Derive the special feature of the gate connecting carry outputs of the half adders to the final carry output of the full adder.

b) What is a MUX? Draw the circuit diagram of a 4-channel MUX using NAND-NAND configuration and use these modules as a full adder. [8+8]

10. Write short notes on <u>any two</u> : [8+8]

a) A differential input differential output amplifier with high input impedance, low output impedance, good CMRR and single gain control facility using not more than two op-amps.

b) Logic circuit of a 2-bit multiplier and 2-bi squarer circuits.

c) Logic circuit of a 4-bit Ripple carry Parallel Adder to add straight binary numbers and development of an 8-bit such adder using above mentioned 4-bit Ripple carry Parallel Adder.

d) TTL NOR gate (2 input) with totempole output and same gate with Open Collector output.

e) CMOS and TTL inverters with 3-state outputs.

f) CMOS MUX-CUM-DMUX circuit (4 channel) for analog and digital signal processing.

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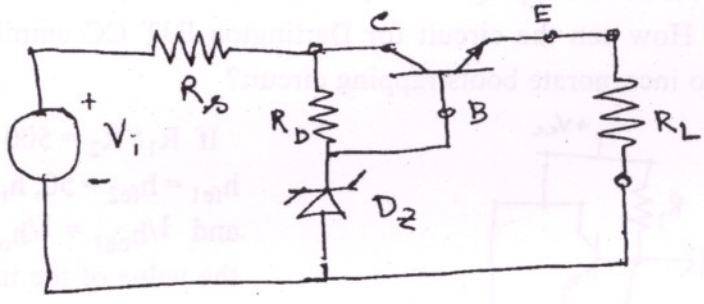

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