Code No: C4EC01 **R05**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
R05 IV B.Tech. (CCC) Supplementary Examinations June – 2009
VLSI TECHNOLOGY AND DESIGN
(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 100

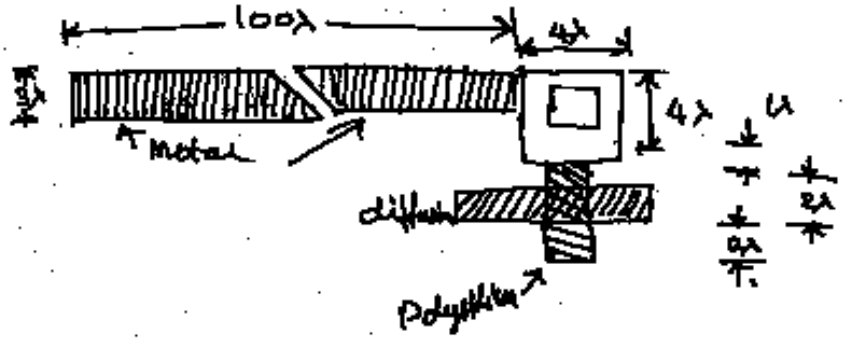
Answer any **FIVE** Questions.
All Questions carries **equal marks**.

1.a) Briefly describe the nMOS fabrication process.
b) Draw a basic inverter circuit and explain its operation for nMOS.
c) Explain the action of BiCMOS inverter circuit. [6+6+8]

2.a) What is twin tub process? Explain where it used.
b) Compare CMOS and Bipolar technologies. [10+10]

3.a) Draw the stick diagram and a mask layout for an 8:1 nMOS inverter circuit. Both the input and output points should be on the polysilicon layer.
b) Write a brief note on inverter delays. [12+8]

4.a) What is sheet resistance model?
b) Calculate the area capacitance value with a structure occupying more than one lay as shown in the figure below. [8+12]



5.a) Draw a clocked inverter circuit and explain its operation.
b) Design a shift register with the dynamic latch operated by a two-phase clock. 8+8

6.a) Design a logic gate network for the full adder using multilevel logic.
b) Design a two bit comparator circuit using two level logic. [10+10]

7.a) A chip core is $3000\lambda \times 2500\lambda$ and requires 0.8A. It needs 18 signal input pads and 19 signal output pads. How many V_{DD} and V_{SS} pads are required assuming a 12λ power ring? Will the total chip size be limited by the chip core or by the pad ring?
b) Explain the two complementary ways to improve clock distribution. [10+10]

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8.a) Explain the fault model in CMOS designs.
b) Write a brief note on layout design to improve testability of a circuit. [10+10]

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