Reg. No. : | | | | | | | | | | | |

Question Paper Code : 11315

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2011

Fourth Semester

Electrical and Electronics Engineering

EE 2255 — DIGITAL LOGIC CIRCUITS

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions

PART A — ($10 \times 2 = 20$ marks)

1. State DeMorgan's theorem.

2. Why is MUX called as data selector?

3. Write the excitation table for JK flip flop.

4. Write the characteristics table for SR flip flop.

5. State the hazards in asynchronous sequential circuits.

6. What is the difference between asynchronous and synchronous sequential circuits?

7. Name the types of ROM.

8. Define fan in and fan out characteristics of digital logic families.

9. What are ASM?

10. When can RTL be used to represent digital systems?

PART B — (5 × 16 = 80 marks)

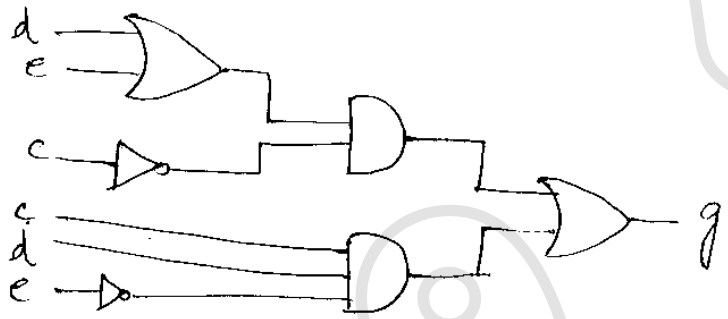
11. (a) (i) Reduce the given expressions using Boolean algebra :

(1) $x'y'z' + x'y'z + x'yz + xy'z + xyz$

(2) $abc' + ab'c + a'bc + abc$

(3) $p'q'r + p'qr' + p'qr + pqr' + pq'r'$. (12)

(ii) For the given circuit, derive an algebraic expression in SOP form : (4)



Or

(b) (i) Reduce the following expression using k-map. (6)

$f = x'y'z + w'xz + wxyz' + wxz + w'xyz$.

(ii) Implement a full adder circuit with

(1) Decoder

(2) Multiplexer. (10)

12. (a) Draw the state diagram. Derive the state equation and draw the clocked sequential circuit for the following state table. (16)

	Next state		Output	
Present state	*x = 0*	*x = 1*	*x = 0*	*x = 1*
AB	AB	AB	Y	Y
00	00	01	0	0
01	11	01	0	0
10	10	00	0	0
11	10	11	0	0

Or

(b) Design BCD counter using T flip flops, where flip flop inputs are TQ_1, TQ_2, TQ_4 and TQ_8. (16)

13. (a) Design an asynchronous BCD counter. (16)

Or

(b) Describe the steps involved in design of asynchronous sequential circuit in detail with an example. (16)

14. (a) (i) Implement the following two Boolean functions with a PLA :

$F_1(A,B,C) = \sum(0,1,2,4)$

$F_2(A,B,C) = \sum(0,5,6,7)$.

(10)

(ii) Describe the characteristics of all types of memories. (6)

Or

(b) (i) Write notes on digital logic families. (9)

(ii) Design ROM for the following functions.

$F_1 = \sum(1,2,3)$; $F_2 = \sum(0,2)$. (7)

15. (a) Write the VHDL code for mod 6 counter. (16)

Or

(b) Describe the RTL in VHDL. (16)

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