Fourth Semester B.E Degree Examination
(Common to CS and IS)

Model Question Paper I

06CS45 Microprocessors

Note: Answer any *FIVE* Full questions, selecting at least TWO Questions from each PART

Time: 3 Hours Maximum marks : 100

PART A

1. a) Explain the internal architecture of 8086 microprocessor with a neat diagram. (10)
b) Explain any five addressing modes with an example for each. (10)

2. a) Explain the following: (12)
i) segment and ends ii) EQU iii) ASSUME iv) ASCII codes
b) Explain briefly Assembler, Linker, Locator and debugger. (8)

3. a) Write a program to find biggest of three numbers. (5)
b) Write a program to add first 8 natural numbers (5)
c) Explain all intersegment jumps along with their instruction formats. (5)
d) Write a delay procedure for producing approximately 5 milliseconds for 8086 microprocessor working at 5Mhz (5)

4. a) Write a program to demonstrate passing parameters to procedures using general memory. (10)
b) Compare macros and procedures. (5)
c) Explain the sequence of events in the stack during a **far call** procedure and **ret** (5)

PART B

5. a) Explain the following instructions with examples. (10)
DAA AAM CMPSB SCASB IDIV
b) Explain the following directives with examples. (10)
DQ EVEN PUBLIC ORG BYTE PTR

6. a) Interface 16k RAM and 32k ROM to 8086 microprocessor using memory chips of size 4k RAM and 4k ROM. Assume suitable starting addresses for RAM and ROM. Use decoders for interfacing. (10)
b) Explain the difference between memory mapped I/O and directed mapped I/O (6)
c) How 8088 microprocessor accesses memory and ports (4)

7. a)Explain the action taken by 8086 when a interrupt occurs . Explain the interrupt vector table. (10)
b) Explain, with the internal block diagram, the 8259A along with all the ICWs and OCWs. (10)

8. a) Explain with the internal block diagram of 8255 the different operational modes and the necessary control words. (10)
b) Explain interfacing 8-digit seven segment display unit to 8086 through 8255 device operating in mode 0 (10)

Fourth Semester B.E Degree Examination
(Common to CS and IS)

Model Question Paper II

06CS45 Microprocessors

Note: Answer any *FIVE* Full questions, selecting at least TWO Questions from each PART

Time: 3 Hours Maximum marks : 100

PART A

1. a) With a neat diagram explain the structure of a microcomputer 08
   b) Explain with an example, the sequence of operations performed when an instruction is being executed by the microprocessor. 08
   c) Briefly discuss the evolution of microprocessors. 04

2. a) Write and Explain the template for MOV instruction. Find the machine code for the following instruction: MOV CS:[BX], AL 10
   b) Find and explain the errors, if there are any, in the following instructions:
      i) MOV BH, AX
      ii) IN AL, 280H
      iii) DIV AL, BL
      iv) PUSH CL
      v) ROR AL, 4 10

3. a) How are the flags of 8086 categorized? Explain each of the flag bits. 10
   b) Write code segments to do the following:
      i) Average of 4 bytes stored in an array 05
      ii) Convert packed BCD byte to two ASCII Characters, each representing a digit in the packed BCD. 05

4. a) What are the sequence of operations that take place when a procedure is called and when the control is returned from the procedure back to calling program? 10
   b) Write a procedure to check whether the password entered is correct or not. (Assume a simple password of 6-10 characters length). 10

PART B

5. a) How do you take care of labels in a MACRO? Give an example. Write a macro to convert the given 2 digit BCD number to corresponding binary. 10
   b) Write a delay loop to produce a delay of approximately 10 milliseconds in a microprocessor working with 10 MHz frequency. 10

6. a) Explain the minimum mode configuration of 8086 with a neat diagram 10
   b) Describe memory-mapped I/O and direct I/O. Give the main advantages and disadvantages of each. 10

7. a) Briefly explain the structure of Interrupt Vector Table with a neat diagram. 08

b) Describe the sequence of actions that an 8259A and an 8086 will take when 8259A receives an interrupt signal on its IR2 input. Assume only IR2 is unmasked in the 8259A and that 8086 INTR input has been enabled with a STI instruction. 12

8 a) Explain the different methods of parallel data transfer. 10

b) Explain the control word register of 8255A in detail. 10