Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER– III (New) EXAMINATION – WINTER 2019**

**Subject Code: 3131704 Date: 26/11/2019**

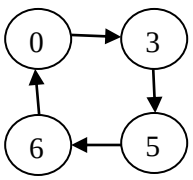
**Subject Name: Digital Electronics**

**Time: 02:30 PM TO 05:00 PM Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

| | | | MARKS |
|---|---|---|---|
| **Q.1** | **(a)** | Give the comparison of 1's and 2's complements. | **03** |
| | **(b)** | Explain De Morgan's theorem with suitable example. | **04** |
| | **(c)** | Explain the commutative law, associative law, and distributive law in Boolean algebra with example | **07** |
| **Q.2** | **(a)** | Convert $(163.875)_{10}$ to binary. | **03** |
| | **(b)** | Design Full Adder using two Half Adder and one two input OR gate. | **04** |
| | **(c)** | Implement the following function with 8:1 multiplexer: F(A, B, C, D)= ∑(0, 1, 3, 4, 8, 9, 15) | **07** |
| | | **OR** | |
| | **(c)** | Explain the working of 4:1 multiplexer. | **07** |
| **Q.3** | **(a)** | What do you mean by universal gates? Implement NOT, AND, OR with any one universal gate. | **03** |
| | **(b)** | Implement 4 bit Shift Register for 1010 binary pattern. | **04** |
| | **(c)** | A combinational circuit is defined by functions: F1 (A,B,C) = ∑m(3, 5, 6, 7) F2 (A,B,C) = ∑m(0, 2, 4, 7) Implement the circuit with PLA having three inputs, four product terms and two outputs. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Explain the operation of master slave J-K flip flop. | **03** |
| | **(b)** | Explain gray code in detail. | **04** |
| | **(c)** | Design a type T counter for given state diagram | **07** |

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|---|---|---|---|
| **Q.4** | **(a)** | Describe Fan In, Noise Margin and Propagation Delay parameters for digital IC. | **03** |
| | **(b)** | xplain ROM with block diagram. Give classification of ROM. | **04** |
| | **(c)** | Design 3 to 8 line decoder with neat sketch and truth table. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Simplify Boolean function F = A'B'C'+B'CD'+A'BCD'+AB'C' using K map. | **03** |
| | **(b)** | Explain TTL gate with Totem pole output. | **04** |

| | | | |
|---|---|---|---|
| | **(c)** | Explain 4 bit magnitude comparator with necessary Boolean expression. | **07** |
| **Q.5** | **(a)** | Explain D flip-flop. | **03** |
| | **(b)** | Explain arithmetic ,logic micro operation. | **04** |
| | **(c)** | Minimize the following function using tabulation method:<br>$F(w, x, y, z) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15)$ | **07** |

**OR**

| | | | |
|---|---|---|---|
| **Q.5** | **(a)** | Design full subtracter with necessary derivation of functions. | **03** |
| | **(b)** | Explain the following register transfer operation with the help of necessary diagram<br>T1: C <------ A<br>T2: C <------ B<br>Assume A, B and C are 4 – bit registers. | **04** |
| | **(c)** | Simplify the Boolean expression $F(A,B,C,D) = \Sigma(2,3,6,7,8,10,11,13,14)$ using K Map. | **07** |

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